Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A method for writing a memory module comprising:
providing a plurality of memory cells, wherein each memory cell stores 2-bit data and comprises a substrate, a P-type drain, a P-type source, a stack dielectric layer, and a gate, and the plurality of memory cells are arranged in a matrix with the gates of the memory cells on the same row being connected to the same word line, the drains of the memory cells on the same column being connected to the same bit line,and the sources of the plurality of memory cells on the same row being connected to the same source line;
applying a source line voltage to the source lines of the plurality of memory cells;
applying a first word line voltage to the word line of the memory cell to be written in order to turn on a P-type channel of the memory cell to be written;
applying a second word line voltage to the word line of the memory cell not to be written in order to turn off the P-type channel of the memory cell;
applying a bit line voltage to the bit line of the memory cell to be written so that a hot hole in the P-type channel of the memory cell to be written induces hot electrons to

be injected into the stack dielectric layer of the memory cell to be written; and
applying a substrate voltage to the substrate of the plurality of memory cells.

[c2] 2.The method of claim 1wherein the source line voltage is larger than the bit line voltage so that the hot hole in the P-type channel of the memory cell to be written induces the hot electrons to be injected into the stack dielectric layer of the memory cell to be written at a place adjacent to the P-type drain to generate first bit data.

[c3] 3.The method of claim 1wherein the source line voltage is less than the bit line voltage so that the hot hole in the P-type channel of the memory cell to be written induces the hot electrons to be injected into the stack dielectric layer of the memory cell to be written at a place adjacent to the P-type drain to generate second bit data.

[c4] 4.The method of claim 1 wherein the matrix is a NOR-array.

[c5] 5.The method of claim 1 wherein the stack dielectric layer is composed of a silicon dioxide layer, a charge storage layer, and another silicon dioxide layer.

[c6] 6.The method of claim 5 wherein the charge storage layer is composed of silicon nitride (Si_3N_4).

[c7] 7.The method of claim 5 wherein the charge storage layer is composed of silicon oxy-nitride ($Si_xN_yO_z$).

[c8] 8.A method for reading a memory module comprising:
providing a plurality of memory cells, wherein each memory cell stores 2-bit data and comprises a substrate, a P-type drain, a P-type source, a stack dielectric layer, and a gate, and the plurality of memory cells are arranged in a matrix with the gates of the memory cells on the same row being connected to the same word line, the drains of the memory cells on the same column being connected to the same bit line,and the sources of the plurality of memory cells on the same row being connected to the same source line;
applying a source line voltage to the source lines of the plurality of memory cells;
applying a first word line voltage to the word line of the memory cell to be read;
applying a second word line voltage larger than the first word line voltage to the word line of the memory cell not to be read;
applying a voltage equivalent to the first word line voltage to the substrates of the plurality of memory cells; and
applying a bit line voltage to the bit line connected to the memory cell to be read in order to enlarge a depletion

region between the P-type drain or the P-type source and the substrate of the memory cell to be read.

[c9] 9.The method of claim 8wherein the source line voltage is less than the bit line voltage in order to enlarge the depletion region between the P-type source and the substrate of the memory cell to be read.

[c10] 10.The method of claim 8wherein the source line voltage is larger than the bit line voltage in order to enlarge the depletion region between the P-type source and the substrate of the memory cell to be read.

[c11] 11.The method of claim 8 wherein the matrix is a NOR-array.

[c12] 12.The method of claim 8 wherein the stack dielectric layer is composed of a silicon dioxide layer, a charge storage layer, and another silicon dioxide layer.

[c13] 13.The method of claim 12 wherein the charge storage layer is composed of silicon nitride (Si_3N_4).

[c14] 14.The method of claim 12 wherein the charge storage layer is composed of silicon oxy-nitride ($Si_xN_yO_z$).

[c15] 15.A method for erasing a memory module comprising: providing a plurality of memory cells, wherein each memory cell stores 2-bit data and comprises a substrate,

a P-type drain, a P-type source, a stack dielectric layer, and a gate, and the plurality of memory cells are arranged in matrix with the gates of the memory cells on the same row being connected to the same word line, the drains of the memory cells on the same column being connected to the same bit line,and the sources of the plurality of memory cells on the same row being connected to the same source line;

applying a word line voltage to the word lines of the plurality of memory cells;

applying a source line voltage larger than the word line voltage to the source lines of the plurality of memory cells; and

applying a voltage equivalent to the source line voltage to the substrates of the plurality of memory cells.

[c16] 16.The method of claim 15 wherein the matrix is a NOR-array.

[c17] 17.The method of claim 15 utilizing Fowler-Nordheim tunneling to erase the electrons limited in the gate.

[c18] 18.The method of claim 15 wherein the stack dielectric layer is composed of a silicon dioxide layer, a charge storage layer, and another silicon dioxide layer.

[c19] 19.The method of claim 18 wherein the charge storage

layer is composed of silicon nitride (Si_3N_4).

[c20] 20.The method of claim 18 wherein the charge storage layer is composed of silicon oxy-nitride ($Si_xN_yO_z$).